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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,659	01/20/2004	Simon C. Steely JR.	200313629-1	9866

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HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
CHERY, MARDOCHEE	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 05/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,659	STEELY ET AL.	
	Examiner	Art Unit	
	Mardochee Chery	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,8-12 and 18-32* is/are rejected.

7)☒ Claim(s) *2-7 and 13-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 8-10, 12, 18-19, 24-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edirisooriya (2003/0195939) in view of Chen (6,931,496).

As per claim 1, Edirisooriya discloses a system comprising: a first node including data having an associated state, the associated state of the data at the first node being a modified state [par. 22, ll 14-16]; and a second node operative to provide a non-migratory source broadcast request for the data [par. 19, ll 5-16], the second node being operative to receive the data from the first node and assign a shared state to an associated state of the data at the second node.

However, Edirisooriva does not specifically teach the first node being operative in response to the non-migratory source broadcast request to provide the data to the second node and to transition the associated state of the data at the first node from the modified state to an owner state without updating memory as required by the claim.

Chen discloses the first node being operative in response to the non-migratory source broadcast request to provide the data to the second node and to transition the associated state of the data at the first node from the modified state to an owner state without updating memory [col.5, ll 5-10, ll 36-42, ll 60 to col. 6, ll 6] to provide a data maintenance method in a distributed shared memory system to efficiently solve the access deadlock problem (col. 3, ll 10-12).

Since the technology for implementing a cache coherency system with transitioning the associated state of the data at the first node from the modified state to an owner state without updating memory was well known as evidenced by Chen, an artisan would have been motivated to implement this feature in the system of Edirisooriva to provide a data maintenance method in a distributed shared memory system to efficiently solve the access deadlock problem. Thus, it would have obvious to one of ordinary skill in the art at the time of invention by Applicant, to modify the system of Edirisooriva to include transitioning the associated state of the data at the first node from the modified state to an owner state without updating memory because this would have provided a data maintenance method in a distributed shared memory system to efficiently solve the access deadlock problem (col. 3, ll 10-12) as taught by Chen.

As per claim 8, Chen discloses the first node is operative in response to the non-migratory source broadcast request to provide a shared data response to the second node [col. 6, ll 1-6].

As per claim 9, Edirisooriya discloses further migration of the data from the second node is precluded when the associated state of the data at the second node is the shared state [par. 33, ll 8-23].

As per claim 10, Chen discloses at least one other node that provides a non-data response to the second node in response to the non-migratory source broadcast request from the second node, the non-data response indicating that the at least one other node does not have a valid copy of the data requested by the second node [col. 7, ll 55-61].

As per claim 12, the rationale in the rejection of claim 1 is herein incorporated.

As per claim 18, the rationale in the rejection of claim 9 is herein incorporated.

As per claim 19, the rationale in the rejection of claim 10 is herein incorporated.

As per claims 24 and 25, the rationale in the rejection of claim 1 is herein incorporated.

As per claim 26, Chen discloses means for selecting one of the XREADM request and XREADN request to broadcast from the first node [Figs. 4 and 5].

As per claim 27, Chen discloses means for predictively selecting one of the XREADM request and XREADN request to broadcast from the first node [Figs. 4 and 5].

As per claim 28, the rationale in the rejection of claim 1 is herein incorporated.

As per claim 29, the rationale in the rejection of claim 1 is herein incorporated.

As per claim 30, the rationale in the rejection of claim 26 is herein incorporated.

As per claim 31, the rationale in the rejection of claim 27 is herein incorporated.

As per claim 32, the rationale in the rejection of claim 1 is herein incorporated.

3. Claims 11 and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edirisooriya (2003/0195939) in view of Chen (6,931,496) and further in view of Cypher (6,484,240).

As per claim 11, Edirisooriya discloses the first node defines a first processor and the second node defines a second processor [Fig. 1], the first and second processors each having an associated cache that comprises a plurality of cache lines [Fig. 1],], the first and second processors being capable of communicating with each other and with a

system memory via an interconnect [Fig. 4], the system further comprising a first cache controller associated with the first processor and a second cache controller associated with the second processor [Fig. 1], the first cache controller being operative to manage data requests and responses for the associated cache of the first processor [Fig. 1], the first cache controller effecting state transitions associated with the data in the associated cache of the first processor based on the data requests and responses for the associated cache of the first processor [Figs. 1, 2, 3], the second cache controller being operative to manage data requests and responses for the associated cache of the second processor [Fig. 1], the second cache controller effecting state transitions associated with the data in the associated cache of the second processor based on the data requests and responses for the associated cache of the second processor [Figs. 1-4].

However, Edirisooriya and Chen do not specifically teach each cache line having a respective tag address that identifies associated data and each cache line having state information that indicates a state of the associated data for the respective cache line as required by the claim.

Cypher discloses each cache line having a respective tag address that identifies associated data and each cache line having state information that indicates a state of the associated data for the respective cache line [col. 1, ll 20-25] to specify the access rights and ownership responsibilities for a corresponding processor (col. 1, ll 23-25).

Since the technology for implementing a cache coherency system with each cache line having a respective tag address that identifies associated data and each cache line having state information that indicates a state of the associated data for the respective cache line was well known as evidenced by Cypher, an artisan would have been motivated to implement this feature in the system of Edirisooriya and Chen in order to specify the access rights and ownership responsibilities for a corresponding processor. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Edirisooriya and Chen to include each cache line having a respective tag address that identifies associated data and each cache line having state information that indicates a state of the associated data for the respective cache line since this would have enabled specifying the access rights and ownership responsibilities for a corresponding processor (col. 1, ll 23-25) as taught by Cypher.

As per claim 20, the rationale in the rejection of claim 11 is herein incorporated.

As per claim 21, the rationale in the rejection of claims 1 and 11 is herein incorporated.

As per claim 22, Chen discloses the source processor further comprises an associated source processor cache having a source processor cache line for storing the data, the source processor cache line having an associated state, the source processor

storing the data in the source processor cache line and assigning a shared state to the associated state of the source processor cache line in response to receiving the S-DATA response from the target processor [coll6, ll 58 to col. 7, ll 17; col. 7, ll 49 to col. 8, ll 3].

As per claim 23, Chen discloses the source processor further comprises an associated source processor cache having a source processor cache line for storing the data, the source processor cache line having an associated state, the source processor storing the data in the source processor cache line and assigning a dirty state to the associated state of the source processor cache line in response to receiving the D-DATA response from the target processor [col. 7, ll 49-61; col. 8, ll 52-67].

Allowable Subject Matter

4. Claims 2-7, 13-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571) 272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manonama Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 14, 2006

Mardochee Chery
Examiner
AU 2188

Mano Padmanabhan
4/17/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER